

What is Claimed is:

1. A nonvolatile ferroelectric memory control device comprising:

5 a page address buffer for latching a page address having a block page address region and a column page address region in response to a chip enable signal, and for decoding the latched page address;

a row address latch unit for latching a row address
10 in response to the chip enable signal, and for outputting the latched row address;

an address transition detector for detecting transition of the latched row address, and for outputting an address transition detecting signal; and

15 a chip control signal generator for selectively generating a control signal to control a chip operation in response to the address transition detecting signal.

2. The device according to claim 1, wherein the
20 page address buffer comprises:

a page address latch unit for latching the page address in response to the chip enable signal, and for outputting the latched page address; and

a page decoder for decoding the latched page address.

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3. The device according to claim 1, wherein the row address is arranged in more significant bit region, a column page address of the page address is arranged in less significant bit region, and a block page address of the page address is arranged between the row address region and the column page address region.

4. A nonvolatile ferroelectric memory control device comprising:

10 a page address buffer for latching a page address having a block page address region and a column page address region in response to a chip enable signal, and for decoding the latched page address;

a row address latch unit for latching a row address in response to the chip enable signal, and for outputting the latched row address;

an address transition detector for detecting transition of the latched row address, and for outputting an address transition detecting signal;

20 a reset signal transition detector for detecting transition of a reset signal in response to the chip enable signal, and for outputting a reset transition detecting signal;

a write enable signal transition detector for detecting transition of a write enable signal in response

to the chip enable signal, and for outputting a write enable transition detecting signal;

a synthesizer for outputting a transition synthesizing signal in response to the address transition
5 detecting signal, the reset transition detecting signal and the write enable transition detecting signal; and

a chip control signal generator for selectively generating a control signal to control a chip operation in response to the transition synthesizing signal.

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5. The device according to claim 4, wherein the row address is arranged in more significant bit region, a column page address of the page address is arranged in less significant bit region, and a block page address of the
15 page address is arranged between the row address region and the column page address region.

6. The device according to claim 4, wherein the page address buffer comprises:

20 a page address latch unit for latching a page address in response to the chip enable signal, and for outputting the latched page address; and

a page decoder for decoding the latched page address.

25 7. The device according to claim 6, wherein the

page address latch unit comprises:

a page address controller for latching the page address in response to the chip enable signal, and for selectively outputting the latched page address; and

5 a first output means for delaying an output signal from the page address controller, and for outputting the latched page address.

8. The device according to claim 4, wherein the
10 row address latch unit comprises:

a row address controller for latching the row address in response to the chip enable signal, and for selectively outputting the latched row address;

a latch controller for latching an output signal from
15 the row address controller in response to a latch control signal, and for selectively outputting the latched output signal; and

a second output means for delaying an output signal from the latch controller, and for outputting the latched
20 row address.

9. The device according to claim 4, wherein the reset signal transition detector comprises:

a reset signal detector for latching a high voltage
25 level while the chip enable signal is disabled before the

reset signal transits to a low level in an initial stage of the memory cell operation; and

a pulse generator for generating the reset transition detecting signal having a pulse width for a predetermined delay time depending on the high voltage level.

10. The device according to claim 9, wherein the reset signal detector comprises:

an input controller for detecting transition of the reset signal and the chip enable signal;

a driver, driven in response to an output signal from the input controller, for selectively outputting a power voltage or a ground voltage; and

a latch unit for latching an output signal from the driver for a predetermined time.

11. The device according to claim 9, wherein the pulse generator comprises:

a delay unit for delaying an output signal from the reset signal detector for a predetermined time; and

a logic unit for performing a logic operation on output signals from the reset signal detector and the delay unit, and generating the reset transition detecting signal.

12. A nonvolatile ferroelectric memory comprising a

plurality of unit blocks,

wherein each unit block comprises a plurality of cell arrays, a plurality of row decoders and a plurality of column pages, and

5 the plurality of column pages in one unit block constitute a unit block page to be activated simultaneously.

13. The memory according to claim 12, wherein each column page comprises:

10 a sense amplifier buffer unit comprising a plurality of sense amplifiers connected one by one to a plurality of bitlines, wherein each of the plurality of sense amplifiers is activated in response to a sense amplifier enable signal;

15 a column selector comprising a plurality of column selecting switches connected one by one to the plurality of sense amplifiers; and

 a data bus unit, connected to the plurality of column selecting switches, for controlling input/output operations
20 of a column selecting signal.

14. The memory according to claim 13, wherein each sense amplifier comprises:

 an activation regulating switch for supplying power
25 to drive a sense amplifier when the sense amplifier enable

signal is activated;

a latch amplification unit for amplifying both nodes of the sense amplifier when the activation regulating switch is activated; and

5 an equalizing unit for initializing both nodes of the sense amplifier when an equalizing signal is activated.

15. The memory according to claim 14, wherein each sense amplifier comprises:

10 a pull-up driver for pulling up a main bitline when a main bitline pull-up signal is activated;

a bitline switching unit for controlling a bitline selecting signal to selectively connect the main bitline to a first node of the sense amplifier;

15 a reference voltage controller for controlling a reference voltage selecting signal to selectively supply a reference voltage to a second node of the sense amplifier;

a column selecting switch for controlling a column selecting signal to selectively connect the data bus unit
20 to both nodes of the sense amplifier;

a write driving switching unit for driving write data applied from the data bus unit, and for outputting the driven data into the column selecting switch;

a read driving switching unit for driving read data
25 applied from the column selecting switch, and for

outputting the driven data into the main bitline; and

a ferroelectric capacitor unit for storing data when the sense amplifier is inactivated, and for restoring the previous data when the sense amplifier is activated.

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16. The memory according to claim 12, wherein in a data access of the plurality of column pages, a sense amplifier is kept active and data stored in the sense amplifier are immediately accessed when transitions of a row address and a reset signal are not detected.

17. The memory according to claim 12, wherein one unit block page further comprises:

a data bus buffer unit comprising a plurality of data bus buffers for buffering data outputted from the plurality of column pages; and

a data input/output buffer unit for buffering input data or output data of the data bus buffer unit.

20 18. A nonvolatile ferroelectric memory comprising:

a plurality of unit blocks each comprising a plurality of cell arrays;

a common data bus unit for exchanging input/output data with the plurality of unit blocks;

25 a unit block page comprising a plurality of column

pages; and

a data bus unit for exchanging input/output data with the unit block page,

wherein the plurality of column pages in the unit
5 block page are activated simultaneously.

19. The memory according to claim 18, wherein each of the plurality of unit blocks comprises the plurality of cell arrays, a main row decoder, a plurality of sub row
10 decoders and a plurality of chip selectors, and

the plurality of sub row decoders are controlled by one main row decoder.

20. The memory according to claim 19, each column
15 page comprises:

a sense amplifier buffer unit comprising a plurality of sense amplifiers connected one by one to a plurality of common data buses, wherein each of the plurality of sense amplifiers is activated in response to a sense amplifier
20 enable signal; and

a column selector comprising a plurality of column selecting switches connected one by one to the plurality of sense amplifiers, wherein each of the plurality of column selecting switches outputs a column selecting signal into
25 the data bus unit.

21. The memory according to claim 20, wherein each sense amplifier comprises:

an activation regulating switch for supplying power
5 to drive a sense amplifier when the sense amplifier enable signal is activated;

a latch amplification unit for amplifying both nodes of the sense amplifier when the activation regulating switch is activated; and

10 an equalizing unit for initializing both nodes of the sense amplifier when an equalizing signal is activated.

22. The device according to claim 21, wherein each sense amplifier comprises:

15 a pull-up driver for pulling up a common data bus when a common data bus pull-up signal is activated;

a common data bus switching unit for controlling a common data bus selecting signal to selectively connect the common data bus to a first node of the sense amplifier;

20 a reference voltage controller for controlling a reference voltage selecting signal to selectively supply a reference voltage to a second node of the sense amplifier;

a column selecting switch for controlling a column selecting signal to selectively connect the data bus unit
25 to both nodes of the sense amplifier;

a write driving switching unit for driving write data applied from the data bus unit, and outputting the driven data into the column selecting switch;

a read driving switching unit for driving read data
5 applied from the column selecting switch, and for outputting the driven data into the common data bus; and

a ferroelectric capacitor unit for storing data when the sense amplifier is inactivated, and for restoring the previous data when the sense amplifier is activated.

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23. The memory according to claim 18, wherein in a data access of the plurality of column pages, a sense amplifier is kept active and data stored in one upper block page are immediately accessed when transition of a row
15 address and a reset signal is not detected.

24. The memory according to claim 18, further comprising:

a data bus buffer unit comprising a plurality of data
20 bus buffers for buffering data outputted from the plurality of column pages, wherein each of the plurality of data bus buffers is connected to the data bus unit; and

a data input/output buffer unit for buffering input data and output data of the data bus buffer unit.

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25. A nonvolatile ferroelectric memory comprising:

a page address latch for latching a page address in response to a chip enable signal;

a row address latch unit for latching a row address
5 in response to the chip enable signal, and outputting the latched row address;

an address transition detector for detecting transition of the latched row address, and outputting an address transition detecting signal;

10 a chip control generator for selectively generating a control signal to control a chip operation in response to the address transition detecting signal; and

a plurality of unit blocks, each unit block comprising a plurality of cell arrays, a plurality of row
15 decoders and a plurality of column pages, wherein the plurality of column pages in one unit block constitute a unit block page to be activated simultaneously.

26. The memory according to claim 25, wherein the
20 page address is divided into a block page address region and a column page address region.

27. A nonvolatile ferroelectric memory comprising:

a page address latch for latching a page address in
25 response to a chip enable signal;

a row address latch unit for latching a row address in response to the chip enable signal, and for outputting the latched row address;

an address transition detector for detecting
5 transition of the latched row address, and for outputting an address transition detecting signal;

a chip control signal generator for selectively generating a control signal to control a chip operation in response to the address transition detecting signal;

10 a plurality of unit blocks comprising a plurality of cell arrays;

a common data bus unit for exchanging input/output data with the plurality of unit blocks;

a unit block page comprising a plurality of column
15 pages; and

a data bus unit for exchanging input/output data with the unit block page,

wherein the plurality of column pages in the unit block page are activated simultaneously.

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28. The memory according to claim 27, wherein the page address is divided into a block page address region and a column page address region.